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Interleaved Switched-Capacitor Bidirectional DC-DC Converter with Wide Voltage-Gain Range for Energy Storage Systems

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ABSTRACT: In this paper, an interleaved switched-capacitor bidirectional dc-dc converter with a high step-up/step-down voltage gain is proposed. The interleaved structure is adopted in the lowvoltage side of this converter to reduce the ripple of the current through the low-voltage side, and the series-connected structure is adopted in the high-voltage side to achieve the high step-up/stepdown voltage gain. In addition, the bidirectional synchronous rectification operations are carried out without requiring any extra hardware, and the efficiency of the converter is improved. Furthermore, the operating principles, voltage and current stresses, and current ripple characteristics of the converter are analyzed. Finally, a 1 kW prototype has been developed which verifies a wide voltage gain range of this converter between the variable low-voltage side (50–120 V) and the constant high-voltage side (400 V). The maximum efficiency of the converter is 95.21% in the step-up mode and 95.30% in the step-down mode. The experimental results also validate the feasibility and the effectiveness of the proposed topology.

KEYWORDS: Bidirectional dc-dc converter, interleaved, switched-capacitor, synchronous rectification, wide-voltage-gain range.

I. INTRODUCTION

WITH the aggravation of the global energy crisis and the deterioration of the environment pollution, the renewable energy systems have become very important in the world [1], [2]. However, the renewable energy systems, including photovoltaic systems and wind-power generating systems, cannot provide a stable power and supply enough instantaneous power when the load power suddenly increases. Energy storage systems, which are used to compensate the power fluctuation between the power generation side and the load side, play an important role in renewable energy power systems [3], [4]. A bidirectional dc-dc converter is a key device for interfacing

There are two different types of bidirectional dc-dc converters in different applications, which include the isolated converters and nonisolated converters. The isolated converters include the flyback, the forward-flyback, the half-bridge, and the fullbridge. High voltage-gain is obtained by adjusting the turns ratio of the high-frequency transformer. However, the leakage inductance of the transformer results in high voltage spikes on semiconductors. In order to reduce the voltage stress caused by the leakage inductance, a full bridge bidirectional dc-dc converterwithaflybacksnubbercircuit[8]andabidirectionaldc-dc converter with an active clamp circuit [9] were proposed. Although the energy of the leakage inductor can be recycled, more additional circuits are required. Besides, when the input and the output voltages cannot match the turns ratio of the transformer, the switching loss will increase dramatically [10].

The nonisolated converters include the Cuk, Sepic/Zeta, coupled inductor, conventional buck-boost, three-level [11]–[14], multilevel, and switched capacitor [15]. Due to the cascaded configurations of two power stages, conversion

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efficiencies of Cuk and Sepic/Zeta are lower [16], [17]. Coupled inductor converters can achieve a high voltage gain by adjusting the turns ratio of the coupled inductor [18], but the problem associated with the leakage inductor is still difficult to be solved and the converter's power converting and transferring capabilities are limited by the capacity of the magnetic core. By utilizing a coupled inductor, the Sepic converter has been modified, and a high efficiency and high voltage-gain bidirectional dc-dc converter with soft-switching was proposed in [19]. But it requires extra active power semiconductors and capacitors. Conventional buck-boost converters are good candidates for low-voltage applications due to their high efficiency and low cost. Unfortunately, the drawbacks including the narrow voltage conversion range, the high voltage stress, and extreme duty cycles of semiconductors make them not suitable for energy storage applications. Though the conventional two-phase interleaved bidirectional dc-dc converter in [20] can reduce low-voltage side current ripples, but this converter still has disadvantages including the narrow voltage conversion range and the high voltage stress for power semiconductors. The voltage stress of power semiconductors of the bidirectional threelevel dc-dc converters in [11] and [12] is half that of the conventional two-phase interleaved bidirectional dc-dc converter, but its voltage-gain range is still narrow. Besides, the low-voltage and high-voltage side grounds of this converter are connected by apower semiconductor, thepotentialdifferencebetweenthetwo grounds is a high-frequency pulse width modulation (PWM) voltage, which may result in more maintenance issues and electromagnetic interference (EMI) problems. The low-voltage and high-voltage sides of the bidirectional three-level dc-dc converter in [14] share the common ground, but the voltage-gain of this converter is still limited. In addition, this converter requires the complicated control scheme to balance the flying capacitor voltage. The converters in [13] and [21] can achieve a high

voltage gain, and the low voltage stress of power semiconductors. However, these converters need more power semiconductors, and require additional hardware circuits and control strategies to maintain the balanced voltage stress of power semiconductors. The switched-capacitor converter structures and control strategies are simple and easy to expand. Different charging and discharging paths of the capacitors transfer energy to either the low-voltage or the high-voltage side to achieve a high voltage gain. Single capacitor bidirectional switched-capacitor converters were proposed in [22] and [23], but the converter's efficiency is low. To reduce the input current ripple, interleaved switched-capacitor converters have been proposed in [24]–[27]. However, the converter in [24] needs more components, and the inductor currents of the converter in are unbalanced when D_b is not equal to $2D_a$. Although the bidirectional dc-dc converters in [26] and [27] just need four semiconductors, the maximum voltage stress of the converter in is that of the high voltage side, and the maximum voltage stress of the converter in [27] is higher than that of the high voltage side. The bidirectional converters in [28] and [29] only require three semiconductors. But their voltage-gain ranges are still small. In addition, the low-voltage and high-voltage side grounds of these converters are connected by a power semiconductor or an inductor, which will also cause extra EMI problems. Finally, the high voltage-gain converter in [30] needs more power components and fails to achieve bidirectional power flows. In addition, the balanced inductor currents just can be achieved when the number of the voltage multiplier stages is odd. The converter in [31] suffers from the huge current ripple in the low-voltage side.

These nonisolated bidirectional dc-dc converters referred above cannot simultaneously achieve the low current ripple, the low voltage stress of power semiconductors, and the wide voltage-gain range. In order to solve this problem, an interleaved switched-capacitor bidirectional dc-dc converter is proposed in this paper. Comparing with the conventional twophase interleaved bidirectional dc-dc converter and the bidirectional three-level dc-dc converter, the proposed converter has advantages including low current ripple, low voltage-stress of power semiconductors, and wide voltage-gain range. In addition, the connection between the low-voltage and the highvoltage side grounds of the proposed converter is a capacitor large enough that each capacitor voltage is considered as constant in each switching period.

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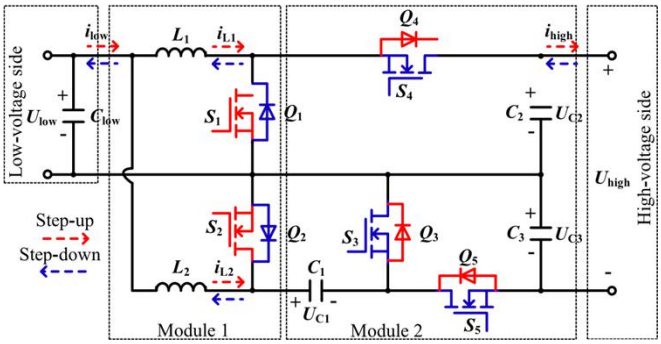

Fig. 1. Proposed topologyof the interleaved switched-capacitor bidirectional dc-dc converter.

rather than a power semiconductor. To achieve a high stepup gain, the capacitors are charged in parallel and discharged in series in the step-up mode. Opposite to the step-up mode, the high step-down ratio can also be obtained because two capacitors are charged in series and discharged in parallel. Furthermore, the capacitor voltage of the proposed converter is half of the high-voltage side voltage, and the efficiency is improved by synchronous rectification operation. This paper is organized as follows. In Section II, the topology of the interleaved switched-capacitor bidirectional dc-dc converter is presented. In Section III, the operating principles of the proposed converter are analyzed in detail. The steady-state characteristics of the converter are analyzed in Section IV and experimental results are analyzed in Section V. Section VI concludes the paper.

II. PROPOSED CONVERTER

The proposed interleaved switched-capacitor bidirectional dc-dc converter is shown in Fig. 1. This converter is composed of four modules. $C_{low}$is the energy storage/filter capacitor of the low-voltage side. Module 1 includes power semiconductors Q_1, Q_2, and energy storage/filter inductors L_1, L_2. In addition, $L_1 - Q_1$ and $L_2 - Q_2$ form the parallel structure of the lowvoltage side. Module 2 is a switched-capacitor network, including switched-capacitor units $C1 - Q3$, $C2 - Q4$, and $C3 - Q5$.

The interleaved structure is used in the low-voltage side of this converter. In this case, the duty cycles of Q_1 and Q_2 are the same, and the phase difference between the gate signals S_1 and S_2 is 180°. The low-voltage side, module 1, module 2, and the high-voltage sideform the bidirectional dc-dcconverter with the structure of the low-voltage side in parallel and the high-voltage side in series.

III. OPERATING PRINCIPLES

To simplify the steady-state characteristics analysis of the proposed converter, several reasonable assumptions about the operating conditions are made as follows: 1) all the power semiconductors and energy storage components of the converter are treated as ideal ones, and the converter operates in the continuous conduction mode; 2) all the capacitances are

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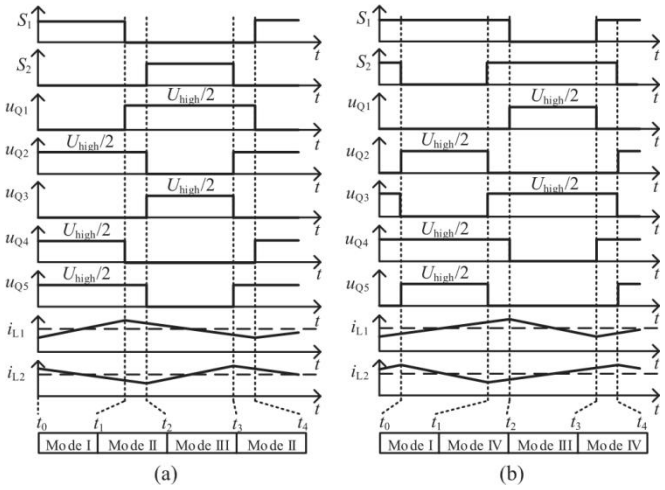

Fig. 2. Typical waveforms of the proposed converter in the step-up mode.

(a) $0 < d\text{Boost} < 0.5$. (b) $0.5 \le d\text{Boost} < 1$.

A. Step-Up Mode

When the energy flows from the low-voltage side to the highvoltage side, the output voltage $U_{high}$is stepped up from $U_{low}$by controlling the power semiconductors of Q_1, and Q_2, and the antiparalleldiodesofQ_3, Q_4,andQ_5.Therelationshipbetween

d_1 and d_2 can be written as $d_1 = d_2 = d_{Boost}$, where d_1 and d_2 are the duty cycles of Q_1 and Q_2, respectively. Fig. 2 shows the
typical waveforms in the step-up mode, and Fig. 3 shows the current flow path of the proposed converter.

Mode I: The power semiconductor Q_1 is turned ON and Q_2 is turned OFF. The antiparallel diode of Q_3 is turned ON, while the antiparallel diodes of Q_4 and Q_5 are turned OFF. The current flow path of the proposed converter is illustrated in Fig. 3(a). The energy is transferred from the dc source $U_{low}$to the inductor L_1. In the meantime, C_1 is being charged by inductor L_2, while C_2 and C_3 are discharging. C_2 and C_3 are connected in series to provide energy for the load in the high-voltage side.

Mode II: The power semiconductors Q_1 and Q_2 are turned OFF. The antiparallel diodes of Q_3 and Q_4 are turned ON, while the antiparallel diode of Q_5 is turned OFF. The current flow path
of the proposed converter is shown in Fig. 3(b). Inductors L_1 and L_2 are discharging. In the meantime, C_1 is charging from inductor L_2, while C_3 is discharging. The dc source U_{low}, L_1, and C_3 output energy to the load.

Mode III: The power semiconductor Q_1 is turned OFF and Q_2 is turned ON. The antiparallel diode of Q_3 is turned OFF, while the antiparallel diodes of Q_4 and Q_5 are turned ON. The current flow path of the proposed converter is shown in Fig. 3(c). Inductor L_1 isdischarging, while L_2 is charged by the dcsource. In the meantime, C_3 is charged by C_1, while C_2 is charged by

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inductor L_1. The dc source U_{low}, L_1, and C_1 output energy to the load.

Mode IV: Power semiconductors Q_1 and Q_2 are turned ON. The antiparallel diodes of Q_3 and Q_4 are turned OFF, while the antiparallel diode of Q_5 is turned ON. The current flow path of the proposed converter is displayed in Fig. 3(d). Inductors L_1

and L_2 are charged by the dc source U_{low}in parallel. In the meantime, C_1 and C_2 are discharging in series to provide energy
for the load.

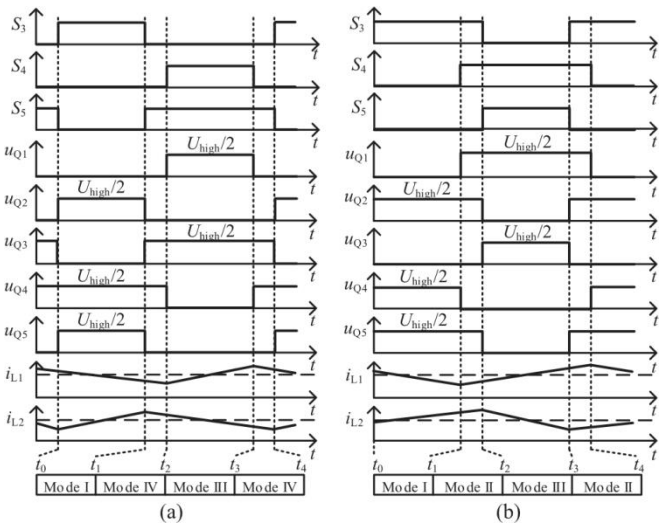

Fig. 4. Typical waveforms of the proposed converter in the step-down mode. (a)0<dBuck<0.5<-dBuck<1

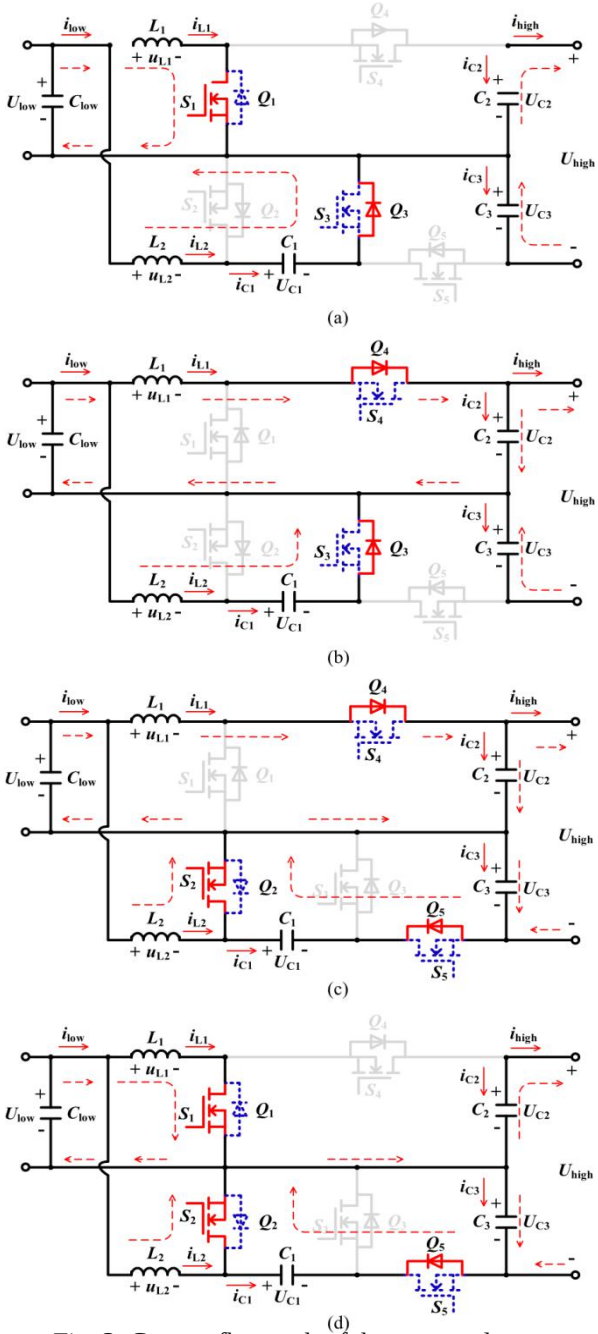

Fig. 3. Current flow path of the proposed converter in the step-up mode. (a)

Mode I $S1S2 = 10$. (b) Mode II $S1S2 = 00$. (c) Mode III $S1S2 = 01$.
(d) Mode IV $S1S2 = 11$.

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C. Synchronous Rectification Operation

As shown in

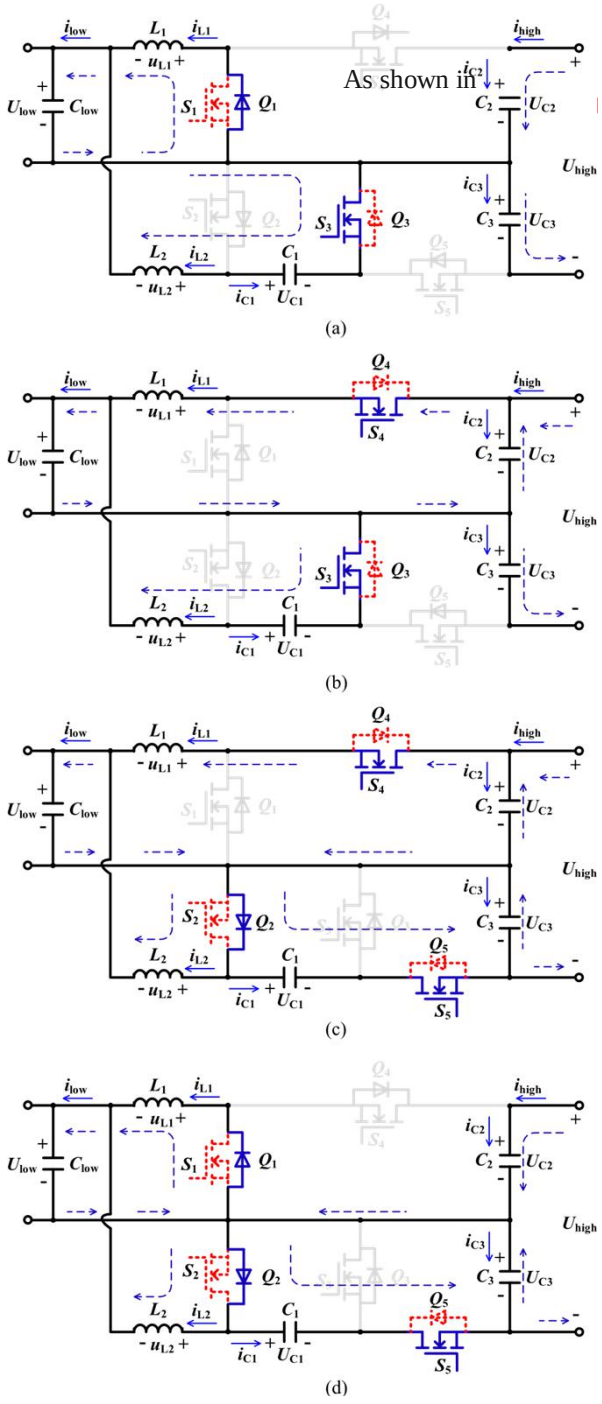

Fig. 1, if the currents of the proposed

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Mode I: The power semiconductor Q3 is turned ON, while Q4 and Q5 are turned OFF. The antiparallel diode of Q1 is turned ON, and the antiparallel diode of Q2 is turned OFF. The current flow path of the proposed converter is shown in Fig. 5(a). C2 and C3
are charged by the dc source Uhighin series. In the meantime, inductors L1, L2, and C1 are discharging to provide energy for the load in the low-voltage side.

Mode II: Power semiconductors Q3 and Q4 are turned ON, while Q5 is turned OFF. The antiparallel diodes of Q1 and Q2 are turned OFF. The current flow path is shown in Fig. 5(b). C1 is discharging to transfer energy to inductor L2, and simultaneously outputting energy to the load. In the meantime, the dc source Uhighcharges L1 and C3, and simultaneously outputs energy to the load. In addition, C2 is discharging to supply energy to L1 and the load.

Mode III: The power semiconductor Q3 is turned OFF, while Q4 and Q5 are turned ON. The antiparallel diode of Q1 is turned OFF, and the antiparallel diode of Q2 is turned ON. The current flow path of the proposed converter is shown in Fig. 5(c). Inductor L2 is discharging to provide energy for the load. In the meantime, the dc source Uhighcharges L1 and C1, and simultaneously provide energy for the load. In addition, C2 is discharging to supply energy to L1 and the load, and C3 is discharging to output energy to C1.

Mode IV: Power semiconductors Q3 and Q4 are turned OFF, while Q5 is turned ON. The antiparallel diodes of Q1 and Q2 are turned ON. The current low path of the proposed converter is shown in Fig. 5(d). L1 and L2 are discharging to provide energy for the load in parallel. In the meantime, the dc source Uhighcharges C1 and C2 in series, and C3 is discharging to supply energy to C1. interleaved switched-capacitor bidirectional converter flow into the corresponding antiparallel diodes, it will result in the lower efficiency, as well as lower utilization of the power semiconductors. Therefore, a high step-up/step-down ratio switched-capacitor bidirectional dc-dc converter with synchronous rectification is proposed further in this paper.

Mode I $S3S4S5 = 100$. (b) Mode II $S3S4S5 = 110$. (c) Mode III $S3S4S5 = 011$.

(d) Mode IV $S3S4S5 = 001$.

The synchronous rectification operating principle of the switched-capacitor bidirectional converter is shown in Fig. 6. In the step-up mode, the main power semiconductors Q_1 and Q_2 switch according to gate signals S_1 and S_2 shown in Fig. 6(a).

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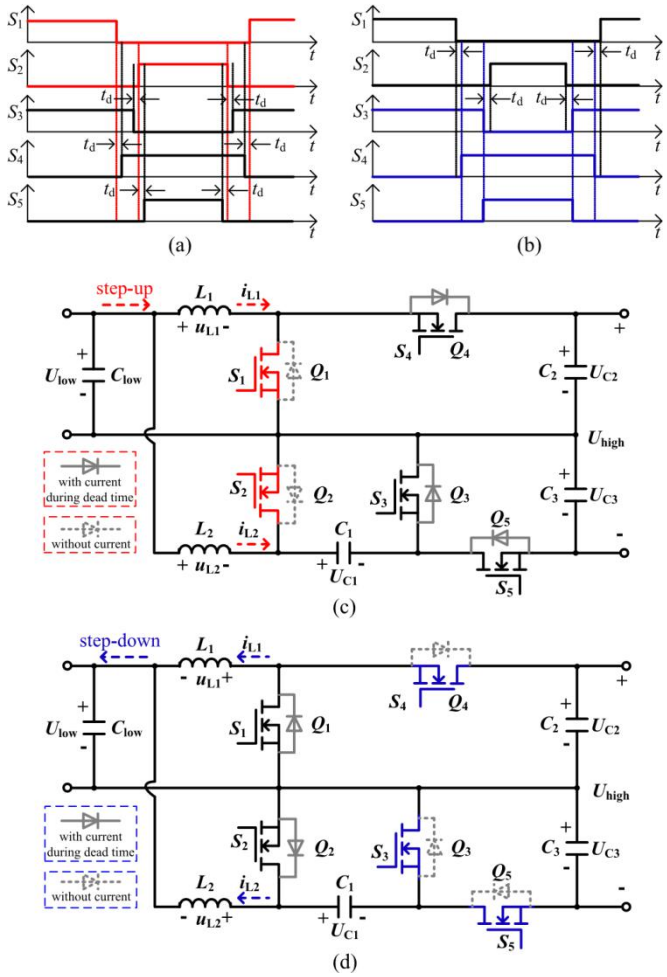

Fig. 6. Synchronous rectification operating principle of the proposed bidirectional converter. (a) Gate signals and the dead time in the step-up mode (left). (b) Gate signals and the dead time in the step-down mode (right). (c) Current flow path in the step-up mode. (d) Current flow path in the step-down mode.

During the deadtimet_d, the current has to fully flow in to the correspo nding antiparallel diodes of Q_3, Q_4, and Q_5. Otherwise, the current may flow into the controlled power semiconductors Q_3, Q_4, and Q_5 due to their lower on-resistances and on-state voltage drops, as shown in Fig. 6(c), by means of the gate signals S_3, S_4, and S_5 shown in Fig. 6(a). Similarly, in the step-down mode, the main power semiconductors Q_3, Q_4, and Q_5 switch according to gate signals S_3, S_4, and S_5 shown in Fig. 6(b). During the dead time t_d, the current also has to fully flow into the antiparallel diodes of Q_1 and Q_2. Otherwise, according to the gate signals S_1 and S_2 shown in Fig. 6(b), the current

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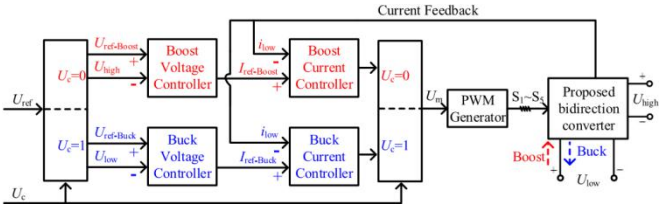

flows into the controlled power semiconductors Q_1 and Q_2, as shown in Fig. 6(d).

Furthermore, the forward voltage drops of the antiparallel diodes are close to zero. As a result, the controlled MOSFETs of the slave active power semiconductors can be turned ON and turned OFF with zero-voltage-switching (ZVS), and the efficiency of the converter is further improved.

D. Control Strategy of Bidirectional Power Flow

Based on the operating principles mentioned above, the bidirectional power flow control strategy can be achieved as shown

Fig. 7. Control strategy of the bidirectional power flows.

in Fig. 7. The voltages $U_{high}$and U_{low}, and the current $i_{low}$are obtained by samplings. The interleaving structure is applied to

reduce the current ripples.

As shown in Fig. 7, the operating modes of the proposed bidirectional dc-dc converter switch between the step-down and the step-up, according to the power flow control signal U_c. It

operates in the step-up mode when $U_c = 0$, the voltage $U_{high}$is controlled by the boost voltage controller with the reference

voltage $U_{ref\text{-}Boost}$ in the voltage-loop. In the meantime, the feedback current $i_{low}$is controlled by the boost current controller with the reference current $I_{ref\text{-}Boost}$ in the current-loop. The corresponding PWM schemes as shown in Figs. 2 and 6(a) are selected to generate the gate signals $S_1 - S_5$ in the step-up mode. Similarly, the converter operates in the step-down mode when $U_c = 1$, the voltage $U_{low}$is controlled by the buck voltage controller with the reference voltage $U_{ref\text{-}Buck}$, and the feedback current $i_{low}$is controlled by the buck current controller with the reference current $I_{ref\text{-}Buck}$, which is in the opposite direction to the reference current $I_{ref\text{-}Boost}$. The corresponding PWM schemes as shown in Figs. 4 and 6(b) are also selected to generate the gate signals $S_1 - S_5$ in the step-down mode.

IV. ANALYSIS OF STEADY-STATE CHARACTERISTICS

A. Voltage-Gain in Steady-State

1) Voltage-Gain in Step-Up Mode: As shown in Figs. 2(a) and 3(c), in the range of $0 < d_{Boost} < 0.5$, C_1 and C_3 are connected in parallel, so that the voltages of C_1 and C_3 are equal.AccordingtoFig.3(a)–(c)andthevoltage-secondbalance principle on L_1 and L_2, the following equations can be obtained

as:

$$\lceil d \times U = (1$$

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$$\begin{cases} d_{\text{Boost}} \times U_{\text{low}} = (1 - d_{\text{Boost}}) \times (U_{C1} - U \end{cases}$$

low) . low . (2)

(1) $U_C1 = U_C3$

Therefore, by simplifying (1), the following equations can be written as:

is

Fig. 9. Experimental prototype of the interleaved switched-capacitor bidirectional dc-dc converter.

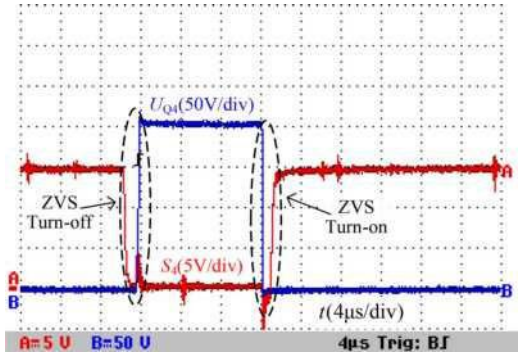

Fig. 11. Gate signal and voltage stress across synchronous rectification power switch $Q4$.

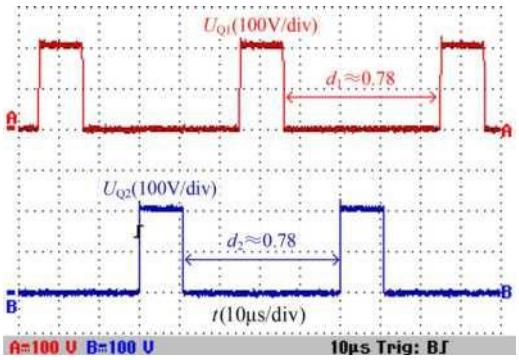

Fig. 12.Voltages $U_{high}$and U_C3 when the input voltage is U_{low}= 50V.

Fig. 10. PWM voltages of power semiconductors $Q1$ and $Q2$. shown in Fig. 9. The experiment parameters are shown in TABLE II.

A. Experimental Results in the Step-Up Mode

The voltage waveforms of the main and slave power semiconductors of the proposed converter in the step-up operation mode are shown in Figs. 10 and 11, respectively. The PWM voltage of each power semiconductors is 200 V, namely

half of U_{high}, which validates the analysis in Section IV. In addition, the current flows through the antiparallel diodes of

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Q_3, Q_4, and Q_5 during the dead time, and the blocking voltages of Q_3, Q_4, and Q_5 are around zero. Otherwise, the controlled MOSFETs Q_3, Q_4, and Q_5 are turned ON and turned OFF with ZVS by the synchronous rectification, e.g., the gate signal S_4 and the voltage stress of Q_4 as shown in Fig. 11.

When the input voltage is U_{low}= 50V, the output voltage to Fig. 12, the voltage across C_3 is 200 V (i.e., half of the output voltage). In addition, the potential difference between the input and output side grounds of this converter is just the voltage across C_3 (i.e., the constant voltage 200 V with very small ripple), rather than the PWM voltage.

The input and inductor currents of the proposed converter in the step-up operation mode are shown in Fig. 13. The inductor currents i_{L1} and i_{L2} are shown in Fig. 13(a). Fig. 13(b) shows the input current $i_{low}$and the inductor current i_{L1}. According to Fig. 13, the current ripple rates of i_{L1} and i_{L2} are about 49%, and the current ripple rate of the input current is only 17.6%. According to (19), the ripple rate of i_{L1} and i_{L2} is 53.57%, and the current ripple rate of $i_{low}$is 17.86% theoretically, which agree with the experimental results. The conclusion that the current ripple of $i_{low}$is much lower than the current ripple of i_{L1} and i_{L2} can be obtained.

The input and capacitor current waveforms of the proposed converter operating in the step-up mode are shown in Fig. 14,

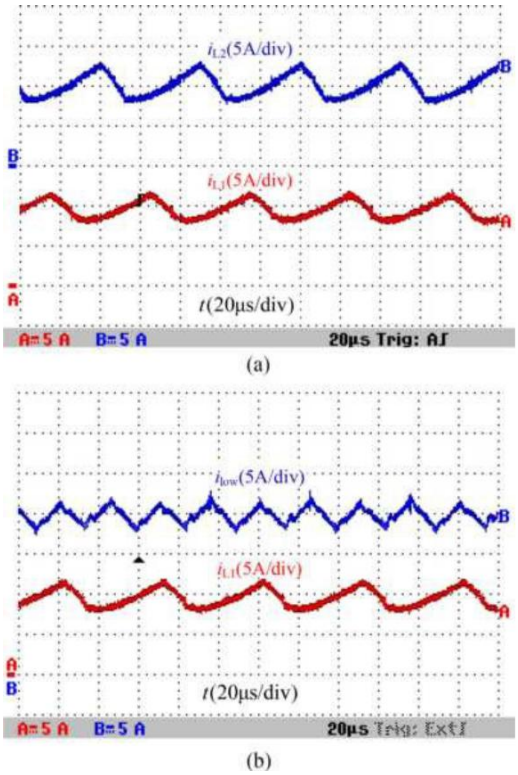

Fig. 13. Input current i_{low}, inductor currents i_L1 and i_L2 when the input voltage is
U_{low}= 50V and the output voltage is U_{high}= 400V. (a) Inductor currents i_L1 and

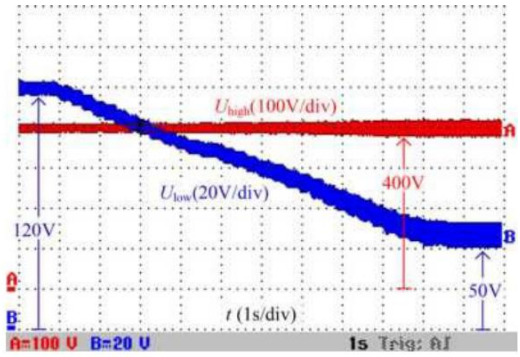

Fig. 15. Output voltage and the wide-range changed input voltage from 120 to 50 V in the step-up mode.

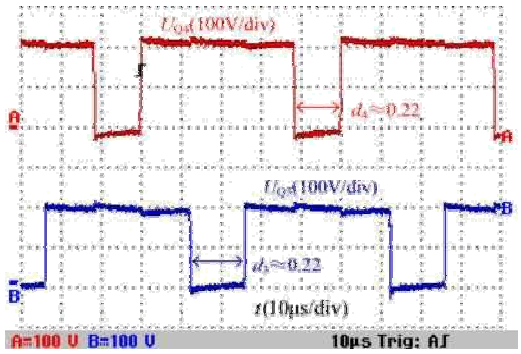

Fig. 16. PWM voltages of power semiconductors $Q3$ and $Q4$.

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i_L2. (b) The input current $i_{low}$and the inductor current i_L1.

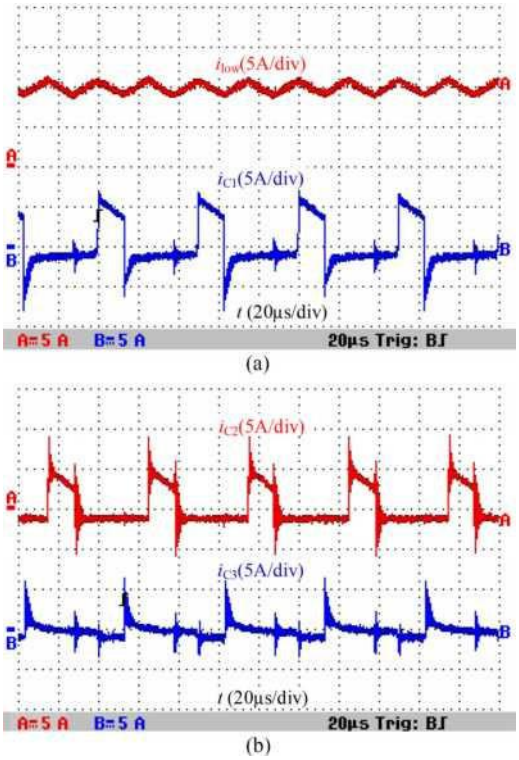

Fig. 14. Input current i_{low}, capacitor currents i_C1, i_C2, and i_C3 in the stepup mode.

(a) The input current $i_{low}$and the capacitor current i_C1. (b) Capacitor currents i_C2 and i_C3.

when the input voltage is U_{low}= 50V and the output voltage is U_{high}= 400V. From Fig. 14, it can be observed that the amplitude of i_{C1} is higher than those of i_{C2} and i_{C3}, and the

maximum charge current of C_1 is nearly equal to half of that of i_{low}. According to Fig. 3(a), the current flowing through Q_3 is the charging current of C_1. Thus, the conclusion that the current stress of Q_3 is reduced to half of the input current can be obtained, which agrees with the theoretical analysis previously mentioned in (16). Besides, the average amplitude of the charging or the discharging current of C_3 is the smallest one (less than 2 A), which is conducive to reduce the voltage fluctuations between the input and output side grounds of this converter.

In the step-up mode, the output voltage can stay constant aroundthereference voltage400Vwiththeactionofthevoltage control loop. Fig. 15 illustrates the dynamical responses of the output voltage and the input voltage when the input voltage is changed from 120 to 50 V continuously. According to Fig. 15, when the input voltage U_{low}varies continuously from 120 to 50 V, the output voltage still stays around 400 V, which means the proposed converter can obtain a wide voltage-gain range varying from 3.3 to 8.

B. Experimental Results in the Step-Down Mode

The voltage waveforms of the main and slave power semiconductors of the proposed converter in the step-down operation mode are shown in Figs. 16 and 17, respectively. Similar to the

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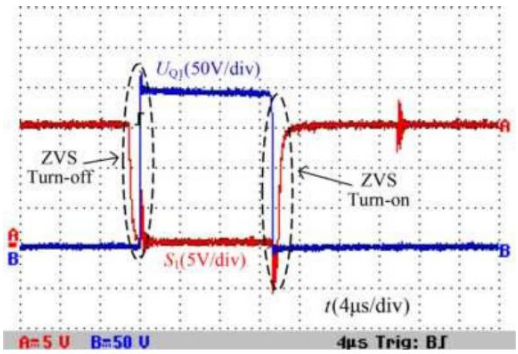


Fig. 17. Gate signal and voltage stress of synchronous rectification power semiconductor $Q1$.

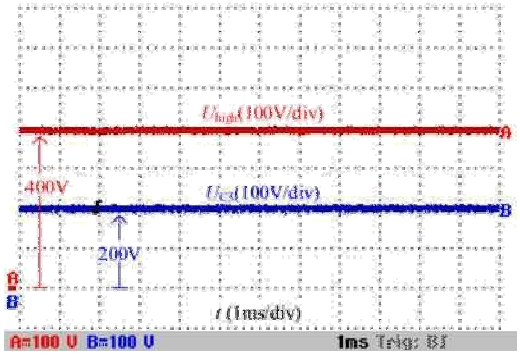
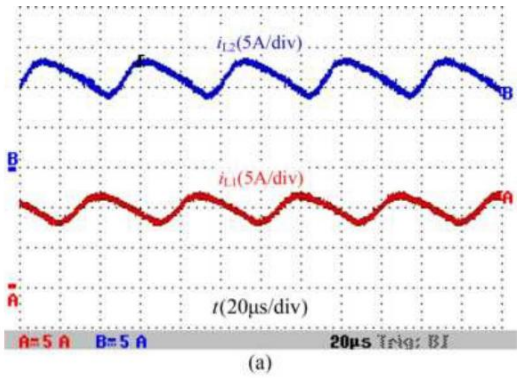
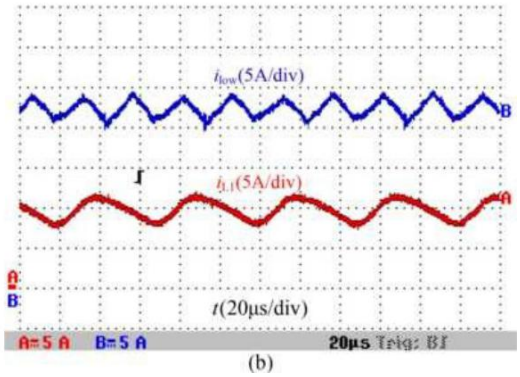


Fig. 18. Voltages $U_{high}$and U_C3 when the output voltage is U_{low}= 50V.



(a)



(b)

Fig. 19. Output current i_{low}, inductor currents i_L1 and i_L2 when the output voltage is U_{low}= 50V and the input voltage is U_{high}= 400V. (a) Inductor currents i_L1 and $iL2$. (b) The output current $i$lowand the inductor current $iL1$.

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experimental results in the step-up mode, the PWM voltage of each power semiconductors is 200 V, which is half of the highvoltage side U_{high}. In addition, the slave power semiconductors Q_1 and Q_2 are also turned ON and turned OFF with ZVS in the synchronous rectification operation, and the gate signal S_1 and the voltage stress of Q_1 are shown in Fig. 17.

When the output voltage is U_{low}= 50V, the input voltage $U_{high}$and the voltage across C_3 are shown in Fig. 18. According to Fig. 18, the voltage across C_3 is also at constant 200 V (i.e.,

half of the output voltage). In addition, the potential difference U_{C3} between the input and output side grounds of this converter also has a very small ripple and dv/dt, which is the same as that in the step-up mode.

The output and inductor current waveforms of the proposed converter in the step-down operation mode are shown in Fig.

19. The inductor currents i_{L1} and i_{L2} are shown in Fig. 19(a). Fig. 19(b) shows the output current $i_{low}$and the inductor current i_{L1}. According to Fig. 19, the current ripple rate of i_{L1} is 46%, and the current ripple rate of i_{L2} is 50.6%. In addition, the current ripple rate of the output current is 17.65%. According to (20), the ripple rate of i_{L1} and i_{L2} is 53.57%, and the ripple rate of $i_{low}$is 17.86% theoretically, which are in accordance with the experimental results. The conclusion that the current

ripple of $i_{low}$is much lower than the current ripple of i_{L1} and i_{L2} can be obtained.

Fig. 20 shows the output and capacitor current waveforms of the proposed converter in the step-down mode, when the

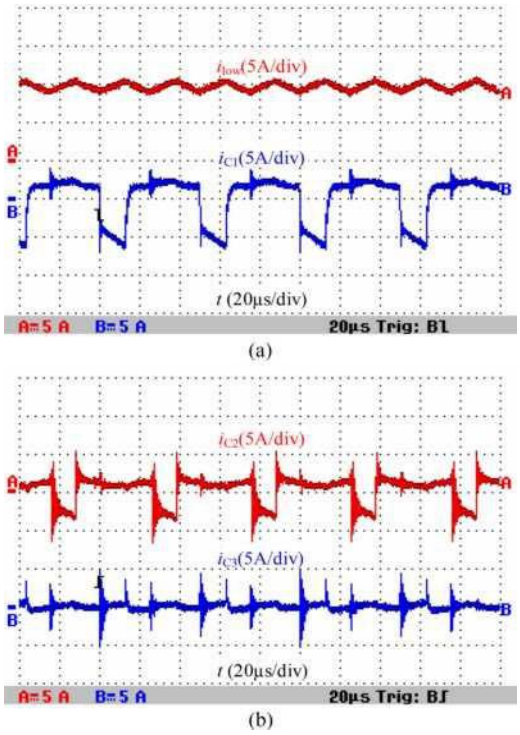

Fig. 20. Output current i_{low}, capacitor currents i_C1, i_C2, and i_C3 in the step-down mode. (a) The output current $i_{low}$and the capacitor current i_C1. (b) Capacitor currents i_C2 and i_C3.

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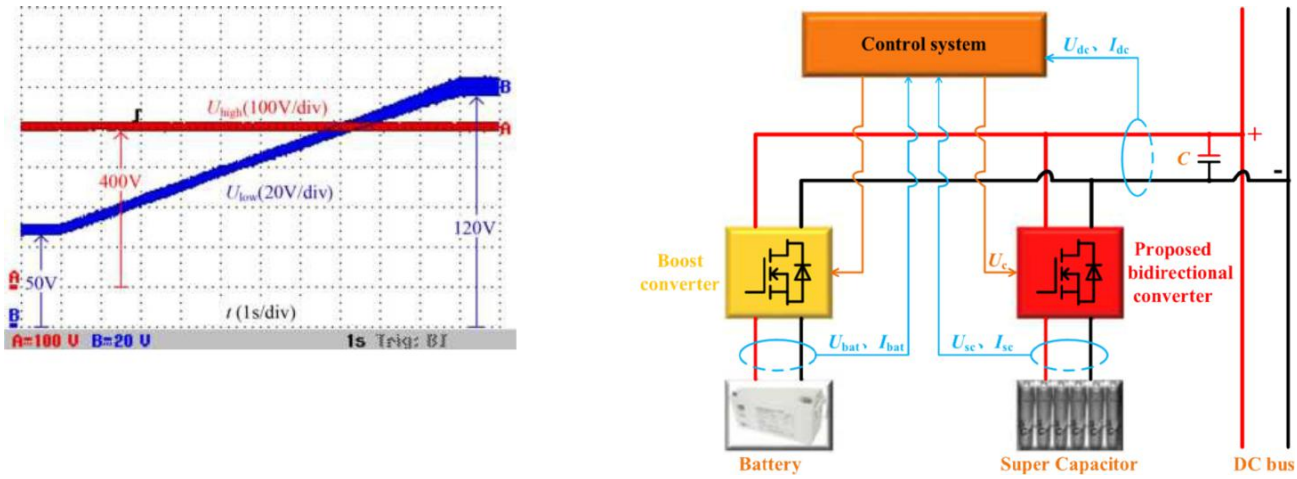

Fig. 21. Input voltage and the wide-range changed output voltage from 50 to 120 V in the step-down mode.

input voltage is U_{high}= 400V and the output voltage is U_{low}= 50V. From Fig. 20, it can be seen that the amplitude of i_{C1} is also

higher than those of i_{C2} and i_{C3}, and the maximum discharging current of C_1 is also nearly equal to half of that of i_{low}. According to Fig. 5(a), the current flowing through Q_3 is the discharging current of C_1. Thus, the conclusion that the current stress of Q_3 is also reduced to half of the output current can be achieved, which also agrees with the theoretical analysis previously mentioned in (17). Besides, the average amplitude of the charging or the discharging current of C_3 is also the smallest one (less than 2 A), which is the same as that in the step-up mode.

Fig. 21 can be used to validate the converter's function of charging the super-capacitors or the batteries. According to Fig. 21, when the input voltage stays around 400 V, the output voltage U_{low}varies continuously from 50 to 120 V under the control of the voltage loop (i.e., a PI controller), in which the reference voltage is adjusted from 50 to 120 V over 10 s, while the input voltage keeps at 400 V. Therefore, it means the proposed converter can obtain a wide voltage-gain range varying from 1/8 to 1/3.3, and it can charge the super-capacitors or the batteries in a wide terminal voltage range.

C. Bidirectional Power Flow Experiment

Fig. 22 shows the hybrid energy sources storage system, where the super-capacitor bank adopts the super-capacitor of CSDWELL's model MODWJ001PM031Z2. In addition, the battery in the hybrid energy sources is a lithium iron phosphate battery with the rated voltage of 48 V. The experimental results of the bidirectional power flow control are shown in Fig. 23.

In the hybrid energy storage sources system shown in Fig. 22,

$U_{dc}$is the dc bus voltage, $U_{bat}$and $I_{bat}$are the output voltage and output current of the battery, $U_{sc}$and $I_{sc}$are the output voltage and
output current of the super-capacitor, and $I_{dc}$is the load current. In the experiment of the bidirectional power flow control, the output voltage of the battery is about 50 V, the output voltage of the super-capacitor is around 40 V, and the dc bus power varies with the step changes from 400 to 650 W. The interleaved switched-capacitor bidirectional dc-dc converter proposed in this paper is applied to interface the super-

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Fig. 22. Hybrid energy sources storage system.

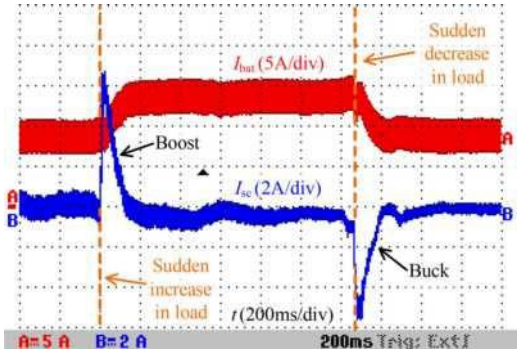

Fig. 23. Experimental results of bidirectional power flow control (supercapacitors are operating).
capacitor and the dc bus, and it operates according to the control strategy shown in Fig. 7.

Fig. 23 shows the variations of $i_{bat}$and i_{sc}during the sudden increase and decrease in the loads of the proposed bidirectional converter, when super-capacitors are operating. According to Fig. 23, when the power required by the dc bus is changed from 400 to 650 W with a step change, the control system sets the control signal $U_c$to "zero." At the same time, the proposed switched-capacitor bidirectional converter responds quickly and operates in the step-up mode. The current I_{sc}increases from zero to 6 A in 20 ms approximately, and the instantaneous power provided by the super-capacitor is nearly equal to the required power change of the dc bus, avoiding the step change current from the battery, which may shorten the life of the battery. As a result, the current of the battery rises from 8 to 13 A gradually, and the current of the super-capacitor falls to zero from I_{sc}= 6A. Similarly, when the power required by the dc bus is changed from 650 to 400 W with a step change, the control system sets the control signal $U_c$to "1." At the same time, the proposed switched-capacitor bidirectional converter responds quickly and operates in the step-down mode. The current I_{sc}increases from zero to 6 A with the opposite direction in 20 ms approximately. As a result, the current from the battery

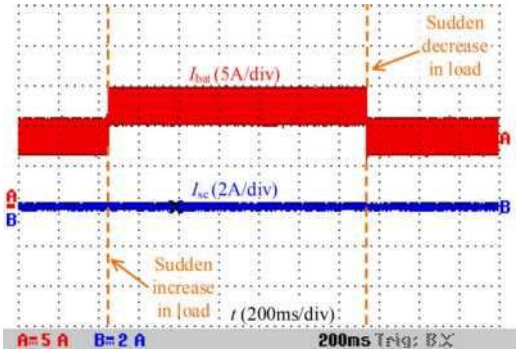

Fig. 24. Experimental results of bidirectional power flow control (supercapacitors are not operating).

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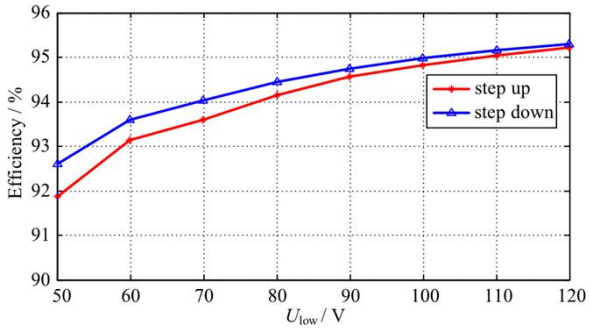

Fig. 25. Efficiencies of the proposed switched-capacitor bidirectional converter in step-up and step-down modes (U_{high}= 400V,U_{low} = 50–120 V,P_n= 1kW).

falls from 13 to 8 A gradually, and the current of the supercapacitor falls to zero from I_{sc}= − 6A.

Fig. 24 shows the variations of $i_{bat}$and $i_{sc}$with the same load stepchange,whensuper-capacitorsarenotoperating.According to Fig. 24, when the dc bus demand power is changed from 400 to 650 W with a step change, the current I_{bat}quickly increases from 8 to 13 A with a step change. When the dc bus demand power is changed from 650 to 400 W with a step change, the current I_{bat}quickly decreases from 13 to 8 A with a step change. It is seen that when the load power varies with a step change, the battery has to tolerate the step change current, and this is easy to cause the impact on the battery itself during the process of the electric vehicle's acceleration and deceleration, and then shorten its service life.

Comparing the experimental results of Figs. 23 and 24, it is seen that when the dc bus demand power quickly increases or decreases, the proposed switched-capacitor bidirectional converter can respond quickly according to the control signal U_c, and the super-capacitor can compensate (take in and send out) the power gap between the battery and the dc bus side to ensure that the current output from the battery changes more slowly and therefore, avoid reduction of the battery life.

The efficiencies of the proposed bidirectional dc-dc converter in the step-up and step-down modes are shown in Fig. 25 when the high-voltage side $U_{high}$is 400 V and the low-voltage side U_{low}varies from 50 to 120 V or 120 to 50 V continuously. The efficiencies are measured by the power analyzer YOKOGAWA/WT3000. According to Fig. 25, the measured efficiencies are from 91.88% (U_{low}= 50V) (U_{low}= 120V) in the step-up mode, and from 92.60% (U_{low}= 50V) to 95.30% (U_{low}= 120V) in the step-down mode. With the constant load P_n= 1kW and U_{high}= 400V in the step-up/down modes, the effective values of the low side currents increase due to the decrease of the low side voltages (i.e., the increase of the voltage-gain). Therefore, the turn-ON/OFF losses and the conduction losses of the power semiconductors will increase, as well as the conduction losses of the equivalent series resistors of thecircuit.Moreover, themaximumefficiency arrivesat95.21% and 95.30% in the step-up and step-down modes, respectively, when the low-voltage side $U_{low}$is 120 V, and the efficiency in the step-down mode is slightly higher than that in the step-up mode.

VI. CONCLUSION

[1] In this paper, an interleaved switched-capacitor bidirectional dc-dc converter has been introduced. The proposed topology can benefit from high step-up/step-down ratio, a wide voltagegain range, and avoiding the extreme duty cycles. In addition, this converter has the advantages of the low voltage stress of power semiconductors and capacitors, and low current ripples in the low-voltage side. Besides, the slave active power semiconductors allow ZVS turn-ONand turn-OFF, and the efficiency of the converter is improved. The capacitor voltages and the inductor currents can be easily balanced due to the self-balance function. The proposed bidirectional dc-dc

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converter has good dynamic and steady-state performance and is suitable for the power interface between the low-voltage battery pack and the high-voltage dc bus for various new energy storage system